CLAIMS

1.	A system for digital system performance enhancement that receives an input signal and a
2	first clock signal, said system comprising:
3 .	clock control logic that receives the first clock signal and generates a second clock signal and
4	a third clock signal, wherein said second and third clock signals have a frequency that this an integer
5	fraction of the first clock signal frequency;
6	a first digital synchronous network responsive to the first clock signal and the input signal,
7	and provides a first output signal;
8	a second digital synchronous network substantially identical to said first digital synchronous
9	network, wherein said second digital synchronous network receives said second clock signal and the
10	input signal, and provides a second output signal;
11	a third digital synchronous network substantially identical to said first digital synchronous
12	network, wherein said third digital synchronous network receives said third clock signal and the
13	input signal, and provides a third output signal; and
14	comparison and selection logic responsive to said first, second and third output signals to
15	determine if a fault has occurred in the computation of said first output signal, wherein if a fault has
16	not occurred said comparison and selection logic provides a system output signal indicative of said
17	first output signal, wherein if a fault has occurred said comparison and selection logic provides said
18	system output signal indicative of said second output signal.